



GCE A LEVEL MARKING SCHEME

SUMMER 2025

**A LEVEL
ELECTRONICS – COMPONENT 2
A490U20-1**

About this marking scheme

The purpose of this marking scheme is to provide teachers, learners, and other interested parties, with an understanding of the assessment criteria used to assess this specific assessment.

This marking scheme reflects the criteria by which this assessment was marked in a live series and was finalised following detailed discussion at an examiners' conference. A team of qualified examiners were trained specifically in the application of this marking scheme. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners. It may not be possible, or appropriate, to capture every variation that a candidate may present in their responses within this marking scheme. However, during the training conference, examiners were guided in using their professional judgement to credit alternative valid responses as instructed by the document, and through reviewing exemplar responses.

Without the benefit of participation in the examiners' conference, teachers, learners and other users, may have different views on certain matters of detail or interpretation. Therefore, it is strongly recommended that this marking scheme is used alongside other guidance, such as published exemplar materials or Guidance for Teaching. This marking scheme is final and will not be changed, unless in the event that a clear error is identified, as it reflects the criteria used to assess candidate responses during the live series.

EDUQAS A LEVEL ELECTRONICS – COMPONENT 2

APPLICATION OF ELECTRONICS

SUMMER 2025 MARK SCHEME

GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

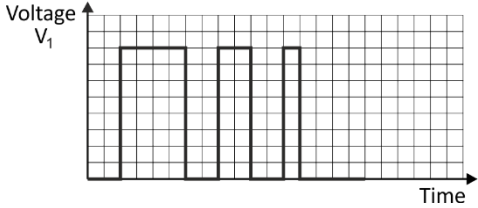
Extended response question

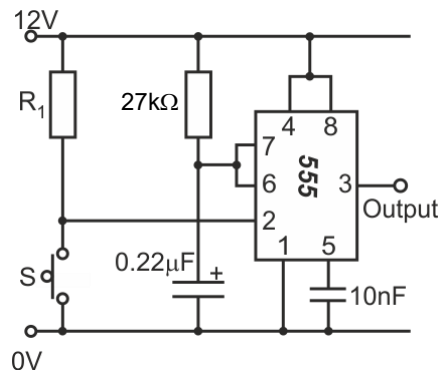
A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

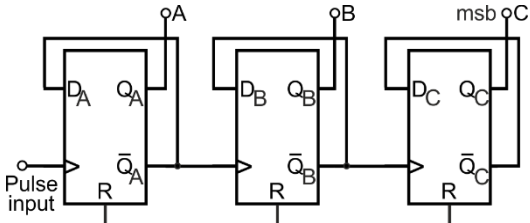
Marking abbreviations

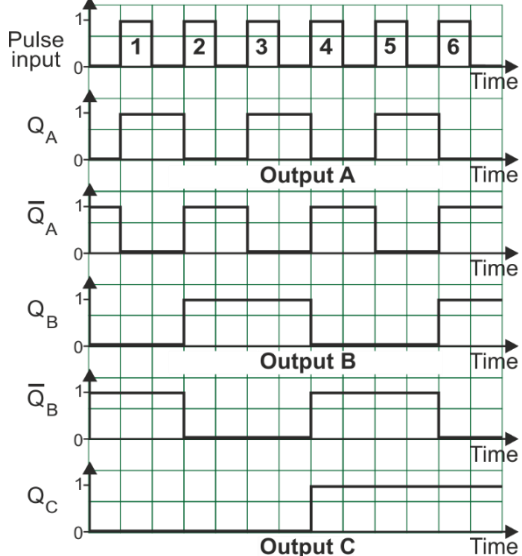
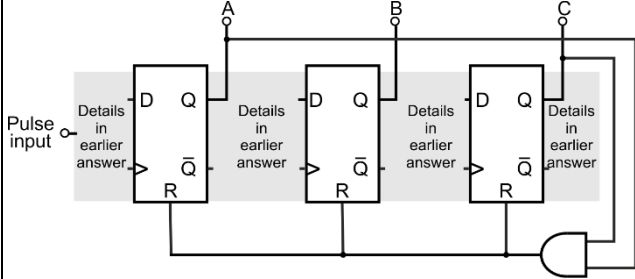
The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

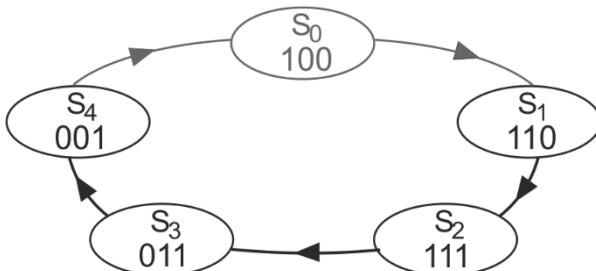
cao	=	correct answer only
ecf	=	error carried forward
bod	=	benefit of doubt

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
1	(a)		 or equivalent Min 2 pulses (timing does not matter) returning to 0V (1) Height – award only if min 2 pulses shown (1)	1	1		2	1
	(b)	(i)	From half-life formula $T = 0.69RC$ $R = \frac{T}{0.69 C} = \frac{5 \times 10^{-3}}{0.69 \times 0.22 \times 10^{-6}} = 32.94 \text{ k}\Omega$ Use of rearranged $T = 0.69RC$ or discharge formula (1) Correct interpretation of multipliers (1) Answer (1) Preferred value = 33 kΩ (ecf) (1)	1	3		4	2
		(ii)	Initial closing of switch charges capacitor to 12V. (1) Capacitor (slowly) discharges through R and instantly returns to 12V every switch bounce (1) but NOT gate input stay at logic 1 for time > duration of switch bounce. (1)	3			3	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(c)		 Trigger sub-system (1) Timing sub-system (1) Rest of circuit (ignoring value of R_1) (1) Use of $T = 1.1RC$ (1) Correct use of multipliers (1) $T = 6.5 \text{ ms}$ (1)	1		5	6	3
			Question 1 total	6	4	5	15	6

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
2	(a)	(i)	 $\overline{Q}$ connected to D (x3) (1) Pulse input connected to first clock Clock connected to previous $\overline{Q}$ (x2) (1) Outputs A, B & C connected to Qs (1)	3			3	
		(ii)	Frequency of signal at X = 15 Hz (1)	1			1	1
		(iii)	Connect 2nd and 3rd stage clock inputs to previous Q outputs. or Use 3 $\overline{Q}$ outputs (2) Connect (all) clock inputs to Q outputs - subtract 1 mark	2			2	

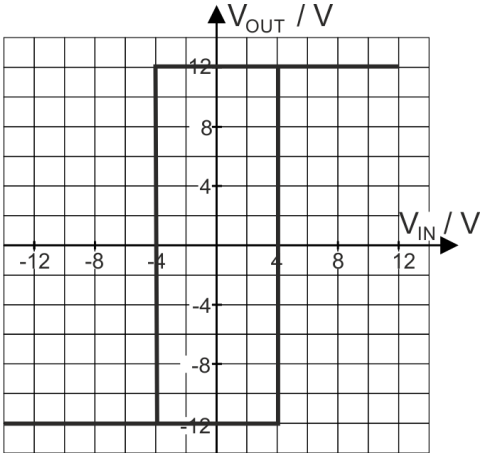
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(b)		Logic level  One mark per correct graph (5) (Ecf from one trace to next) -1 mark max for incorrect pulse height	1	4		5	3
	c	i	The count progresses through the system, one bit at a time.(or equivalent) (1)	1			1	
		ii	Ripple counter can produce false counting at high pulse input frequencies. (1)	1			1	
	d		 Use of A and C outputs (1) Use of AND gate (1) AND gate output to all three resets (1)		3		3	1
Question 2 total				9	7	0	16	5

Question			Marking details	Marks available																																																				
				AO1	AO2	AO3	Total	Maths																																																
3	(a)		 Completely correct (1)	1			1																																																	
	(b)		<table><tr><th rowspan="2">State</th><th colspan="3">Current state</th><th colspan="3">Next state</th></tr><tr><th>C</th><th>B</th><th>A</th><th>D_C</th><th>D_B</th><th>D_A</th></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>2</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>3</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>4</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table> All correct (1)	State	Current state			Next state			C	B	A	D _C	D _B	D _A	0	1	0	0	1	1	0	1	1	1	0	1	1	1	2	1	1	1	0	1	1	3	0	1	1	0	0	1	4	0	0	1	1	0	0	1			1	
State	Current state				Next state																																																			
	C	B	A	D _C	D _B	D _A																																																		
0	1	0	0	1	1	0																																																		
1	1	1	0	1	1	1																																																		
2	1	1	1	0	1	1																																																		
3	0	1	1	0	0	1																																																		
4	0	0	1	1	0	0																																																		
	(c)	(i)	Correct Karnaugh map or Boolean algebra (1) $D_C = \overline{A} + \overline{B}$ (1)		2		2	2																																																
		(ii)	Correct Karnaugh map or Boolean algebra (1) $D_B = C + \overline{A}$ (1)		2		2	2																																																
		(iii)	Correct Karnaugh map or Boolean algebra (1) $D_A = B + \overline{C} . \overline{A}$ (1)		2		2	2																																																

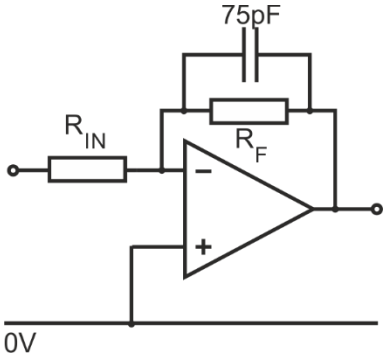
Question			Marking details				Marks available																																				
							AO1	AO2	AO3	Total	Maths																																
	(d)		<table><tr><th rowspan="2">State</th><th colspan="3">Current state</th><th colspan="3">Next state</th></tr><tr><th>C</th><th>B</th><th>A</th><th>D_C</th><th>D_B</th><th>D_A</th></tr><tr><td>5</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>6</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>7</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	State	Current state			Next state			C	B	A	D _C	D _B	D _A	5	0	0	0	1	1	1	6	0	1	0	1	1	1	7	1	0	1	1	1	0	All unused states identified (1) 'Next state' - correct for each (1) x 3 (3) ecf from c - Karnaugh map	1	3		4	3
State	Current state				Next state																																						
	C	B	A	D _C	D _B	D _A																																					
5	0	0	0	1	1	1																																					
6	0	1	0	1	1	1																																					
7	1	0	1	1	1	0																																					
	(e)	(i)	<pre>graph TD; S0((S0 100)) --> S1((S1 110)); S1 --> S2((S2 111)); S2 --> S3((S3 011)); S3 --> S4((S4 001)); S4 --> S0; 101((101)) --> S1; 000((000)) --> S2; 010((010)) --> S2</pre>	Ecf from (d) All correct (1) (ignoring state numbering) 000 & 010 feeding into 111 101 feeding into 110		1		1																																			
		(ii)	No stuck states (or equivalent) (1) Unused states may delay start of main sequence (or equivalent) (1)					2		2																																	
			Question 3 total				3	12	0	15	9																																

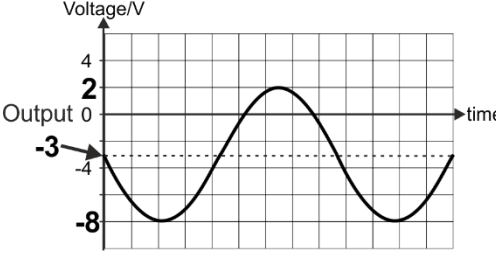
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
4	(a)	(i)	Switch is connected to bit 4 (1)		1		1	
		(ii)	Selects memory bank 1 (1) Configures the TRIS register rather than the port itself (or equivalent.) (1)	2			2	
	(b)		140 <i>check</i> btfss PORTA,4 (allow ecf from (a)(i)) (2) 141 <i>goto</i> <i>check</i> 142 bsf PORTB,6 (2) 143 <i>call</i> <i>onsec</i> 144 <i>bcf</i> <i>PORTB,6</i> 145 <i>call</i> <i>onsec</i> 146 goto <i>check</i> (2) (allow <i>btfss/btfsc</i> <i>PORTA,4</i>)		6		6	5
	(c)	(i)	130 <i>movlw</i> <i>b'1xx1xx0x'</i> (1) <i>x = don't care</i> 131 <i>movwf</i> <i>INTCON</i> (1)		2		2	2
		(ii)	100 <i>panic</i> bsf PORTB,6 ; switch on buzzer (1) 101 btfsc PORTB,0 ; re-test sensor (1) 102 goto panic ; continue alarm (1) 103 <i>bcf</i> <i>INTCON,1</i> ; clear interrupt flag 104 <i>retfie</i> ; return to main program		3		3	3
			Question 4 total	2	12	0	14	10

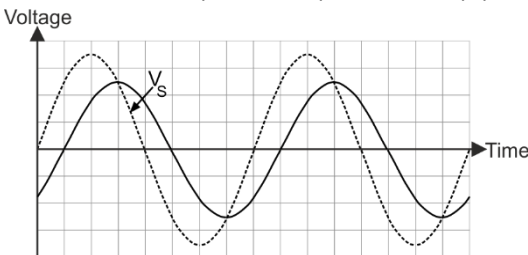
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5	(a)	(i)	Using resolution = $\frac{\text{input voltage range}}{2^n}$ (1) Resolution = $\frac{10}{2^{10}} = 9.766$ or 9.8 mV (accept 10mV) (1) (or equivalent)	1	1		2	1
		(ii)	7.5kHz > 2 x highest signal frequency (1)	1			1	
		(iii)	Time interval between samples = $\frac{1}{\text{sampling frequency}}$ (1) $\frac{1}{7500} = 133\mu\text{s}$ (1) PISO register outputs one bit in time = $\frac{1}{\text{PISO frequency}} = 0.769 \mu\text{s}$ (1) PISO register outputs one 10 bit sample in 10 x 769 ns = 7.69 μs (1) No. of channels using TDM = $\frac{133}{7.69} = 17.3$ (1) = 17 (as answer must be a lower integer) (1) Or equivalent correct method.	2	4		6	4
	(b)	(i)	Block A is the Schmitt trigger (1)	1			1	
		(ii)	Output will always be in saturation / 2 voltage thresholds (1) Small fluctuations in signal level due to noise are ignored / noise spikes are unlikely to breach both thresholds and cause an extra output pulse. (1)		2		2	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		(iii)	When $V_{OUT} = +12V$, and V_{IN} is at the threshold, voltage across R_2 ($3.6k\Omega$) is $12 - 0 = 12 V$ so voltage across R_1 ($1.2k\Omega$) is $\frac{12}{3} = 4 V$ (1) so at first input threshold $V_{IN} = -4 V$ (1) When $V_{OUT} = -12V$, and V_{IN} is at the other threshold, voltage across R_2 ($3.6k\Omega$) is $-12 - 0 = -12 V$ so voltage across R_1 ($1.2k\Omega$) is $\frac{12}{3} = -4 V$ (1) so at second input threshold $V_{IN} = 4 V$ (1)  Correct saturation levels (1) Correct thresholds (allowing ecf. and including shape) (1)	3	3		6	3
			Question 5 total	8	10	0	18	8

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6	(a)		X is a power amplifier (1)	1			1	
	(b)	(i)	Overall voltage gain = 40×40 (1) = 1600 (1)	1	1		2	1
		(ii)	Same voltage gain optimises overall bandwidth. (1)	1			1	
		(iii)	I Using voltage gain = $1 + \frac{R_F}{R_1}$ (1) $R_F = 39 \text{ k}\Omega$ (1) II Capacitor C prevents DC signals reaching the preamplifier (1) III The resistor allows a path for the decoupling capacitor to discharge. (1)	2	2		4	2
	(c)		Using the voltage divider formula $V_2 = \frac{V_1}{R_{OUT} + R_{IN}} \times R_{IN} \quad (1) = \frac{600}{180 + 900} \times 900 = 500 \text{ mV} \quad (1)$	2			2	2
	(d)	(i)	Filter is treble cut / low-pass (1)	1			1	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		ii	 Capacitor in parallel with resistor (1) Capacitor in feedback circuit (1) Rest of circuit correct (1) $\text{Use of } f_b (7\text{kHz}) = \frac{1}{2\pi RC} \quad (1)$ $R_F = 300 \text{ k}\Omega \quad (1)$ $R_F / R_{IN} = 30 \quad \text{or} \quad R_{IN} = 10 \text{ k}\Omega \quad (1)$ E24 Resistors $\geq 1 \text{ k}\Omega \quad (1)$			7	7	3
	e		$\text{SNR} = 10 \log \frac{P_{\text{sig}}}{P_{\text{noise}}} = 10 \log \left(\frac{195.5 - 0.36}{0.36} \right) \quad (2) \text{ -1 if no subtraction of 0.36}$ $= (+) 27.3 \text{ dB} \quad (1)$	1	2		3	2
			Question 6 total	9	5	7	21	10

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
7	(a)	(i)	$V_{OUT} = -R_F \left(\frac{V_A}{R_A} + \frac{V_B}{R_B} \right) = -15 \left(\frac{8}{30} + \frac{6}{30} \right) \quad (1)$ $= -7 \text{ V} \quad (1) \quad \text{(Omission of '-' sign -1 mark)}$	1	1		2	2
		(ii)	 Correct phase (1) Correct amplitude (1) Correct DC level (1)		3		3	3
		(iii)	Clipping occurs first at $V_{OUT} = -12 \text{ V}$ when $V_A = +10 \text{ V} \quad (1)$ $V_{OUT} = -R_F \left(\frac{V_A}{R_A} + \frac{V_B}{R_B} \right) \quad (1)$ $V_B = -R_B \left(\frac{V_{OUT}}{R_F} + \frac{V_A}{R_A} \right) = -30 \left(\frac{-12}{15} + \frac{10}{30} \right) \quad (1)$ $= 14 \text{ V} \quad (1) \quad \text{Accept -14V}$	1	3		4	3
	(b)		Using $V_{OUT} = -\frac{R_F}{R_B} \times 10 \quad (1)$ When $V_R = 0 \Omega$, $V_{OUT} = -5 \text{ V} \quad (1)$ When $V_R = 120 \text{ k}\Omega$, $V_{OUT} = -1 \text{ V} \quad (1) \quad \text{(Omission of '-' sign -1 mark)}$ Range of voltages is -1V to -5 V	1	2		3	2
			Question 7 total	3	9	0	12	10

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
8	(a)	(i)	I Minimum current through R = 2mA (1) II Maximum voltage across R = 11.4V (1) III Voltage at X = 0V → 1V (1) Accept value between 0 and 1.	2	1		3	
		(ii)	Minimum current through thyristor = 7mA (1)	1			1	
		(b) (i)	Graph 1 shows signal across triac (1)	1			1	
		(ii)	Period of mains supply = $\frac{1}{50} = 0.02\text{s} = (8 \text{ squares})$ (1) 1 square = 0.0025s (1) Graph 1 shows 'on' time = 6 squares per cycle = 6 x 0.0025 (1) = 0.015s per cycle (1)	1	3		4	3
		(iii)	I Phase angle $\phi = 45^\circ$ so $\tan \phi = 1$ (1) From $\tan \phi = \frac{R}{X_C}$, $R = X_C = \frac{1}{2\pi fC}$ (1) $R = 31.8\text{k}\Omega$ (31,831 Ω) (1) II  Sine wave with amplitude smaller than V_s (1) Timing (V_C delayed by one square) (1)	2	3		5	5
			Question 8 total	7	7	0	14	8

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
9	(a)	(i)	Line regulation is important as the national grid mains supply voltage varies (with demand). (1)	1			1	
		(ii)	Load ...when the output/load current changes. (1)	1			1	
	(b)	(i)	When V_{OUT} falls, V_2 (or V_-) falls (1) V_1 (or V_+) remains fixed by the zener (1) Hence $(V_+ - V_-)$ increases (1) and so V_3 increases, pushing V_{OUT} ($=V_3 - 0.7$) back up (1)	1	3		4	
		(ii)	Smallest output when R_2 is minimum. (1) Using $V_L = V_Z \left(1 + \frac{R_F}{R_1} \right)$ (1) Smallest output = $15 \left(1 + \frac{0}{100} \right) = 15V$ (1)	2	1		3	1

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			Indicative content: Calculations: $V_{\text{peak}} = 16 \text{ V}$ Voltage across capacitor = $16 - 1.4 = 14.6 \text{ V}$ Voltage across 150Ω resistor = $14.6 - 12 = 2.6 \text{ V}$ When the voltage regulator is working properly: Current through 150Ω resistor = $\frac{2.6}{150} = 17 \text{ mA}$ Maximum base current available = $17 - 10 = 7 \text{ mA}$ Maximum collector current = $7 \times 120 = 0.84 \text{ A}$. This does not achieve the 1amp required. Max. power dissipated in zener = $12 \times 17 = 204 \text{ mW}$. Hence Zener power rating is fine. Max power dissipated in 150Ω resistor = $3.6 \times 17 = 61.2 \text{ mW}$ The resistor power rating is fine. Improvement to achieve spec. Any of: Use a transistor with a greater value of h_{FE}. Decrease value of 150Ω resistor. Change transformer to one having a higher secondary voltage.			6	6	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			5-6 marks A detailed analysis of the system is given. Most of the calculations outlined above are evaluated correctly. <i>There is a sustained line of reasoning which is coherent, relevant, substantiated and logically structured.</i> 3-4 marks At least 4 of the calculations identified above are evaluated and appropriate conclusions made. <i>There is a line of reasoning which is partially coherent, largely relevant, supported by some evidence and with some structure.</i> 1-2 marks The performance of the system is discussed in qualitative terms only. At least 1 calculation is evaluated correctly. <i>There is a basic line of reasoning which is not coherent, largely irrelevant, supported by limited evidence and with very little structure.</i> 0 marks No attempt made or no response worthy of credit.					
			Question 9 total	5	4	6	15	1

Electronics A Component 2 (FR3) version

SUMMARY OF MARKS ALLOCATED TO ASSESSMENT OBJECTIVES

Question	AO1	AO2	AO3	TOTAL MARK	MATHS
1	6	4	5	15	6
2	9	7	0	16	5
3	3	12	0	15	9
4	2	12	0	14	10
5	8	10	0	18	8
6	9	5	7	21	10
7	3	9	0	12	10
8	7	7	0	14	8
9	5	4	6	15	1
TOTAL	52	70	18	140	67