



GCSE MARKING SCHEME

SUMMER 2025

**GCSE
ELECTRONICS – COMPONENT 1
C490UA0-1**

About this marking scheme

The purpose of this marking scheme is to provide teachers, learners, and other interested parties, with an understanding of the assessment criteria used to assess this specific assessment.

This marking scheme reflects the criteria by which this assessment was marked in a live series and was finalised following detailed discussion at an examiners' conference. A team of qualified examiners were trained specifically in the application of this marking scheme. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners. It may not be possible, or appropriate, to capture every variation that a candidate may present in their responses within this marking scheme. However, during the training conference, examiners were guided in using their professional judgement to credit alternative valid responses as instructed by the document, and through reviewing exemplar responses.

Without the benefit of participation in the examiners' conference, teachers, learners and other users, may have different views on certain matters of detail or interpretation. Therefore, it is strongly recommended that this marking scheme is used alongside other guidance, such as published exemplar materials or Guidance for Teaching. This marking scheme is final and will not be changed, unless in the event that a clear error is identified, as it reflects the criteria used to assess candidate responses during the live series.

GCSE ELECTRONICS
COMPONENT 1 – DISCOVERING ELECTRONICS
SUMMER 2025 MARK SCHEME
GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

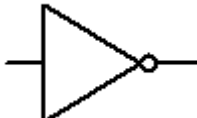
A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

Marking abbreviations

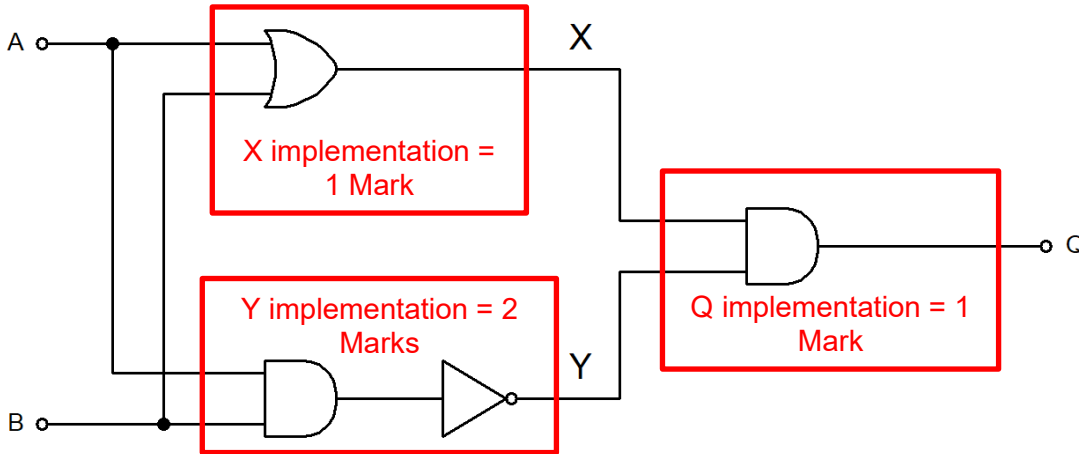
The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

cao = correct answer only

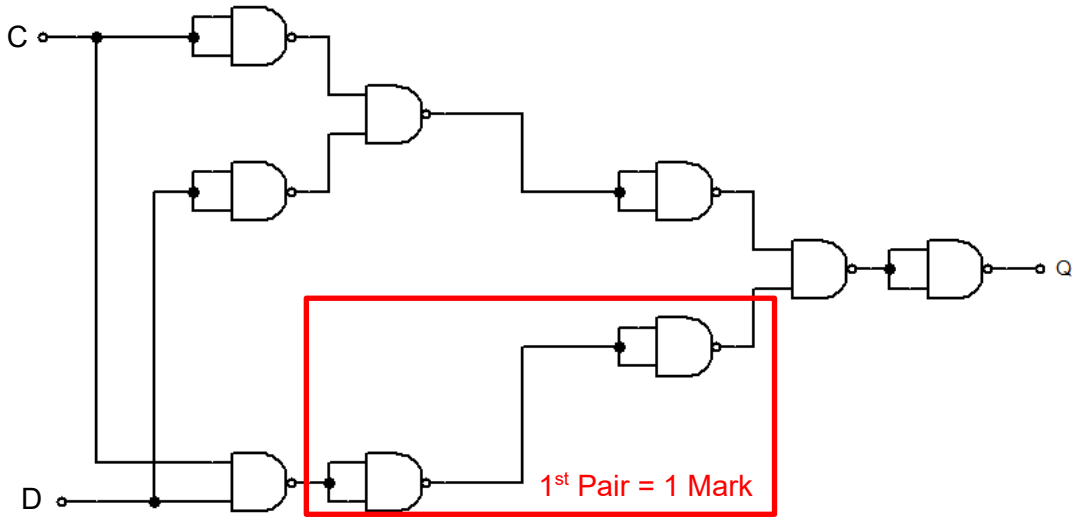
ecf = error carried forward

Question			Marking details	Marks available																												
				AO1	AO2	AO3	Total	Maths																								
1	(a)	(i)	 1 mark	1			1																									
		(ii)	 1 mark	1			1																									
	(b)	<table border="1"><thead><tr><th>B</th><th>A</th><th>X</th><th>Y</th><th>Q</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr></tbody></table> 1 mark for each correct output column. (allow e.c.f. for correct Q from incorrect X or Y)	B	A	X	Y	Q	0	0	1	0	0	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	3		3	
B	A	X	Y	Q																												
0	0	1	0	0																												
0	1	0	0	1																												
1	0	1	0	0																												
1	1	0	1	0																												
	(c)	OR gate		1			1																									

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(d)		$\overline{C + D} = \bar{C} \cdot \bar{D}$ ☒ 1 Mark $\overline{C + D} = \bar{C} \cdot \bar{D}$ ☐ $\overline{C \cdot D} = \bar{C} + \bar{D}$ ☒ 1 Mark $\overline{C + D} = \bar{C} + \bar{D}$ ☐ $\overline{C \cdot D} = \bar{C} \cdot \bar{D}$ ☐ -1 mark for each additional tick.	2			2	
			Question 1 total	5	3	0	8	0

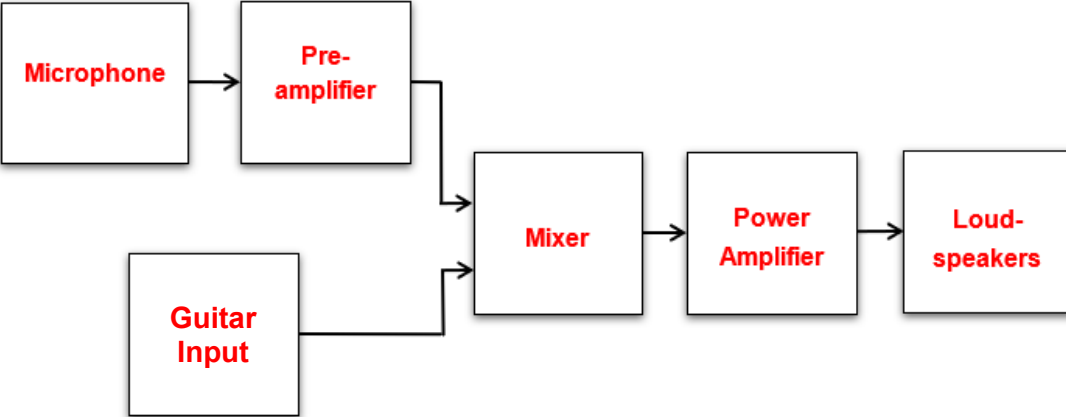
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
2	(a)	(i)	OR gate	1			1	
		(ii)	NAND gate	1			1	
		(iii)	 1 mark for output X gate +connections 2 mark for output Y gate made from AND and NOT gate 1 mark for output Q gate +connections or alternative solution giving correct Q using only AND, OR and NOT gates (4).			4	4	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
2	(b)	(i)	OR Gate = 1 Mark AND Gate = 1 Mark NOR Gate = 1 Mark	3			3	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(b)	(ii)	 1st Pair = 1 Mark		1		1	
	(c)		Either To reduce the number of i.c. packages required (– smaller footprint on circuit boards). or To reduce the cost of projects (as only one type of logic gates needs to be purchased).			1	1	
			Question 2 total	5	1	5	11	0

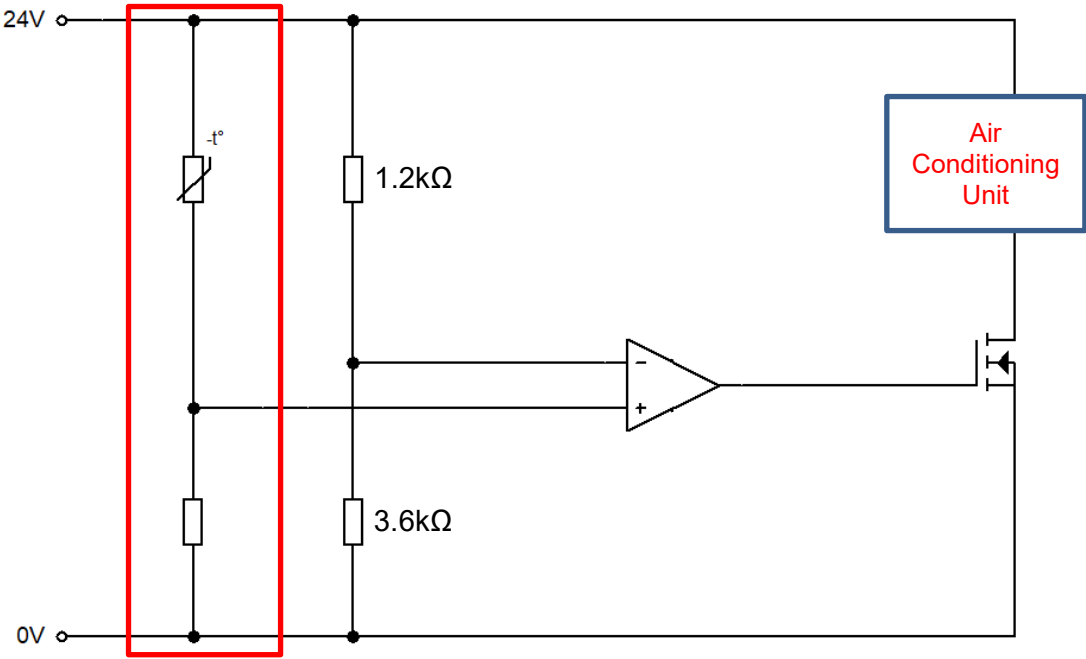
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
3	(a)	(i)	$V_1 = 6 - 2(1) = 4V$ (1)	1	1		2	1
		(ii)	$V = IR$ (1 – Formula) $I_1 = \frac{V}{R}$ (1 – Rearranging) $I_1 = \frac{4}{200}$ (1 – Substitution) ecf on V_1 $I_1 = 20mA$ (1 – Answer)	1	3		4	4
		(iii)	$I_2 = I_3 - I_1$ (1) = 30mA – 20mA ecf = 10mA (1)		2		2	1
	(b)		$V_2 = V_1 = 4V$ (1) ecf – same value as V_1 from answer (a)(i)	1			1	0
	(c)		$V = IR$ $R_2 = \frac{V_2}{I_2}$ (1 – Rearranging) $R_2 = \frac{4}{10 \times 10^{-3}}$ (1 – Substitution / 1 Multiplier) ecf on V_2 from (b), I_2 from (a)(iii) $R_2 = 400\Omega$ (1 – Answer)	1	3		4	4
	(d)		Red (1) Black (1) Brown (1) Gold (1)	4			4	0
			Question 3 total	8	9	0	17	10

Question			Marking details			Marks available				
						AO1	AO2	AO3	Total	Maths
4	(a)		Input sub-system	Processing sub-system	Output sub-system	3	0	0	3	0
			Light sensing unit	Latch unit	Solenoid unit					
			Moisture sensing unit	NOR gate	Buzzer Unit					
				Comparator						
				MOSFET						
				Delay unit						
			1 mark for each correct column							
	(b)		Light Sensing Unit NOT gate Switch Unit OR gate Transistor Switch LED Lights 1 mark for each correct subsystem Accept alternative: Switch unit to NOT gate to NAND Light sensing unit to NAND			0	0	5	5	0

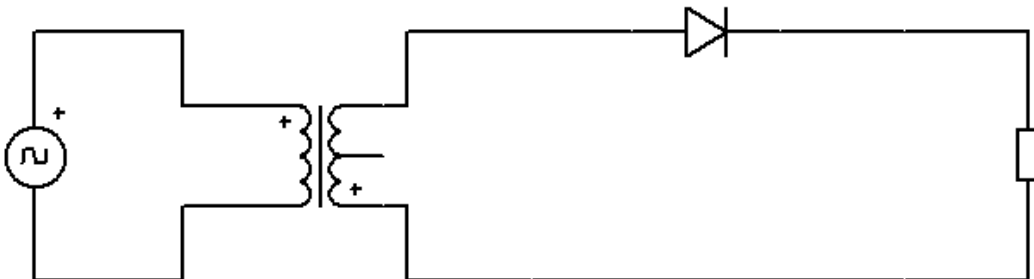
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(c)	(i)	 4 Correct = 3 Marks 3 Correct = 2 marks 2 Correct = 1 mark	3	0	0	3	0
	(c)	(ii)	 1 mark for use of mixer 1 mark for guitar input 1 mark for system connected with all other sub-systems correct.	2	1	0	3	0
Question 4 total				8	1	5	14	0

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5	(a)		$I_Z = 530\text{mA} - 500\text{mA} (1) = 30\text{mA} (1)$	1	1	0	2	2
	(b)		$V_{13} = 12\text{V} - 5.1\text{V} (1) = 6.9\text{V} (1)$ or $V_{13} = 530 \times 13 (1) = 6.9\text{V} \text{ or } 6.89\text{V} (1)$	1	1	0	2	2
	(c)		$P = I^2 R (1 - \text{formula})$ $P = (530 \times 10^{-3})^2 \times 13 (1 - \text{substitution / multiplier})$ $P = 3.6517\text{W} (1 - \text{answer})$ Or $P = I \times V (1 - \text{formula})$ $P = 530 \times 10^{-3} \times 6.9 (1 - \text{substitution / multiplier})$ ecf on V from (b) $P = 3.657\text{W} (1 - \text{answer})$ Or $P = V^2 / R (1 - \text{formula})$ $P = 6.9^2 / 13 (1 - \text{substitution / multiplier})$ ecf on V from (b) $P = 3.662\text{W} (1 - \text{answer})$ A 5W (ecf on calculation of P) resistor would be suitable (1 – choice)	1	3	0	4	4

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(d)	(i)	5.1V (1)	1	0	0	1	0
		(ii)	$13.4 - 5.1 = 8.3\text{V}$ (1)	0	1	0	1	0
			Question 5 total	4	6	0	10	8

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6	(a)		26k Ω ($\pm$ 1k Ω if supported by lines on graph)		1		1	1
	(b)		 Thermistor and Resistor between power rails – 1 Mark Thermistor on top – 1 Mark Centre connection to non-inverting input – 1 Mark		3		3	0

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6	(c)		$V_{OUT} = \frac{R_2}{R_1 + R_2} \times V_{IN}$ ----- (1 Formula) $V_2 = \frac{3.6k}{1.2k + 3.6k} \times 24$ ----- (1 Substitution) $V_2 = 18V$ ----- (1 Answer)	1	2		3	3
	(d)		$I_D = g_M(V_{GS} - 3)$ ----- (1 – equation) $g_M = \frac{I_D}{(V_{GS} - 3)}$ ----- (1 – rearrangement) $g_M = \frac{12}{(22 - 3)}$ ----- (1 – substitution) $g_M = \frac{12}{19} = 0.632S$ (1 - answer)	1	3		4	4
			Question 6 total	2	9	0	11	8

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
7	(a)			1			1	
	(b)		B – 1 mark C – 1 mark -1 mark for any additional ticks		2		2	
Question 7 total				1	2	0	3	0

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
8			Indicative Content: The output driver is correctly configured to switch on the lamp so no circuit changes are required. When the transistor is just saturated there will be 9V across the lamp, and the current through it will be $I = P/V$, = 18/9 = 2A. This gives a required base current of $I_B = I_C/h_{FE} = 2/200 = 0.01\text{A}$ or 10mA. When logic system output is 7 V the voltage across the resistor will be 7 - 0.7=6.3V, the current through it would then be $I = V/R = 6.3 / 820 = 7.68\text{mA}$. The required current is 10mA and therefore the lamp will not be fully illuminated. The value of R needs to be reduced to $R = V / I = 6.3 / 0.01 = 630\Omega$ to provide the correct current, so a 620Ω resistor from the E24 series would be the correct value to allow the circuit to work properly. Alternatively, a transistor with a higher $h_{FE} > 261$ could be used. 5-6 marks Candidates have evaluated the specification fully e.g. all parts of the specification considered against the given circuit, justifying values and connection of components in the design and given a comprehensive description of changes that should be made. Description has a logical thought process and presentation. <i>There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument.</i>	2	4	0	6	4

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			3-4 marks Candidates have evaluated most of the specification e.g. two of the three parts of the specification with the given circuit, justification of values and connection of components in the design may be less clear and given a brief description of changes that should be made. Description has a reasonable thought process and presentation. <i>There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information not relevant to the argument.</i> 1-2 marks Candidates have evaluated little of the specification e.g. one of the three parts of the specification with the given circuit, justification of values and connection of components in the design may be weak and limited description of changes that should be made. Description has a random presentation. <i>There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument.</i> 0 marks No evaluation of circuit against specification or any statement of value. <i>Response not creditworthy or not attempted.</i>					
			Question 8 total	2	4	0	6	4
			PAPER TOTAL	35	35	10	80	30

Summary of marks allocated to assessment objectives

Question	AO1	AO2	AO3	Total	Maths
1	5	3	0	8	0
2	5	1	5	11	0
3	8	9	0	17	10
4	8	1	5	14	0
5	4	6	0	10	8
6	2	9	0	11	8
7	1	2	0	3	0
8	2	4	0	6	4
TOTAL	35	35	10	80	30